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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
05/13/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/499,720	MORRIS ET AL.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the 103 rejection of claims 1-23 have been fully considered but are not persuasive.

Regarding the reference to Jensen, Applicant argues that "The Jensen Patent also fails to teach or suggest a privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level. In addition, there is no teaching or suggestion for one skilled in the art to combine the cache memory of the Arora Patent with the permission bits of the Jensen Patent... Using the permission bits of the Jensen Patent in the cache memory of the Arora Patent would render the system of the Arora Patent inoperable for its intended purpose. If the instructions stored in instruction memory 36 of the Arora Patent were read protected, they could not be processed in the pipeline 32 as required by the Arora Patent. If a page of instruction memory 36 of the Arora Patent were write protected, then nothing could be written to that page of instruction memory 36 from a main memory and instructions could not be stored for processing in the pipeline 32."

The examiner disagrees.

Jensen discloses a cache memory, 16 or 18, including various protection levels (protection and control information included in that tag fields) wherein the individual pages of the cache memory may be write or read protected (Col. 1, lines 45-54; Col. 5, lines 30-54; and Col. 6, line 55 – Col. 7, line 12). In this system, the cache memory includes a page of memory not writeable by applications at a first privilege level since a

page of the cache memory may be write protected. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to provide the protection bits, as disclosed by Jensen, since doing so allows the system to identify particular memory pages as write protected thus, preventing unauthorized modification of programming and providing security against viruses attacking the program code. Although applicant notes that using permission bits in the cache memory of Arora would prevent instructions from being processed and would prevent the storing of instructions into the instruction memory, the reference to Jensen simply teaches that some of the pages of the cache memory may be write or read protected. Therefore, the permission bits would only prevent reading or writing into specific pages. In implementing the system in this manner, the instruction memory of Arora may still be used as intended.

Regarding Applicant's arguments, the examiner maintains that Applicant bases most of his arguments on the labels being given by the Arora patent to the various privilege levels it employs. The Examiner would like to explain that regardless of what the privilege levels are labeled as by the Arora Patent, the examiner is free to interpret the true meaning and relationship of these privilege levels within the system of Arora. Furthermore, the examiner maintains that the terms "future" and "current", as used by the Arora patent, are relative terms and for the purpose of interpretation, the examiner would like to point out that a "future" privilege level can be considered to be the "current" privilege level being prepared for execution in the near future and that a "current"

privilege level can be considered to be the “previous” privilege level of the previously executed instruction.

Applicant further argues that the terms “future” and “current”, used by Arora, are absolute terms and a future privilege level can never be considered to be a current privilege level and the current privilege level can never be considered to be the previous privilege level; similar to if today is Wednesday (i.e., the current day), then it cannot ever be considered to be Thursday (i.e., a future day) or Tuesday (i.e., the previous day). The examiner does not agree with Applicant’s interpretation of the terms in question. The term “current” and “future” are not names for the privilege levels whereas "Wednesday" and "Thursday" represent names of the days. On the other hand, "current" and "future" are labels being given to the privilege levels based on the current time. Since time changes, what is now a future privilege level will become the current privilege level once the future arrives. Similarly, what is now a current privilege level will become a past privilege level once the future arrives. This analysis is similar to the labels "today" and "tomorrow". Once "tomorrow" arrives (which is equivalent to the future) it will become "today". Similarly, once "tomorrow" becomes “today”, as explained above, the day previously labeled as “today” will become “yesterday”.

Additionally, the examiner maintains that the claims as presented do not limit the claim language since the limitations do not provide a clear relationship between the "current" and "previous" privilege levels. Since the claim language does not differentiate

the privilege levels by defining what the “previous” privilege level is previous to or by defining what makes the "current" privilege level current; the examiner is free to interpret these relative terms as it has been explained above. Applicant argues that this interpretation is incorrect because the terms “current” and “previous” are absolute terms that are well defined in the specification and claims. However, the definition provided of these terms does not provide a relationship between the terms such as clearly defining what the previous privilege level is previous to, etc. Therefore, the definition of the term, as provided, still allows for the examiner's interpretation of the terms.

Applicant argues that the Arora patent does not teach reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level since in the Arora patent a previous privilege level state is not stored and therefore cannot be read. However, the Examiner maintains that the previous privilege level state is stored in CPL 38 since a **prior** instruction would have set the CPL 38 to the proper privilege level and the CPL is maintained (stored) in the processor's register set. Then the CPL is compared to the privilege level of the EPC in the process of determining if the fetched instruction requires the processor to change the privilege level from a first level to a second level (Col. 5, lines 40-50).

Applicant argues that the privilege level of the EPC instruction does not teach or suggest the current privilege level. Rather, the EPC instruction directs the processor to

change the privilege level of the CPL and provides a future privilege level, not the current privilege level. Applicant notes that the CPL is the current privilege level, not the previous privilege level state, and the privilege level of the EPC instruction is a future privilege level, not the current privilege level as submitted by the examiner. However, as interpreted by the examiner and regardless of the labels being given to the respective privilege levels of the invention, at the moment of comparison, the privilege level of EPC is the privilege level necessary for the instruction that is **currently** being prepared for execution in the system (instruction requiring a higher priority level follows in the pipeline), thus it is a **current** privilege level. Also, at the moment of comparison, the CPL is the previous privilege level because it was the privilege level set by a prior instruction (Col. 4, lines 19-28), and it is the privilege level that was necessary for the execution of an instruction that was executed previous to the instruction corresponding to the EPC. Therefore, for interpretation purposes, at the moment of privilege level comparison, the EPC represents the current privilege level and the CPL represents the previous privilege level. With this in mind, Arora does teach comparing the read previous privilege level state to the current privilege level.

Applicant mentions that the CPL remains the current privilege level during the execution of the EPC instruction and it is therefore, the current privilege level and not the previous privilege level. However, the privilege level was set by a previous instruction and so, it is considered to be a previous privilege level. Once the CPL is updated when the EPC is executed, the CPL will take on the value of the EPC and will

become the new previous privilege level since it was set by the previous instruction. The new EPC will become the new current privilege level.

Applicant argues that the Arora patent does not teach comparing a read previous privilege level state to the current privilege level state. However, Arora teaches comparing the CPL to the EPC wherein the CPL is stored in the CPL register 38 and must be read from there in order to perform the comparison.

Applicant argues that the Arora patent does not disclose promoting the current privilege level to a second privilege level, which is higher that the first privilege level if the previous privilege level state is equal to or less privileged that the current privilege level. However, as maintained by the examiner, when the CPL and the EPC are compared, if the previous privilege level, which is stored in the CPL, is set to a lower privilege level (less privileged) than the current privilege level, indicated by the EPC (CPL is set to level 3 and EPC is set to level 0, Col. 6, lines 46-61) then, the current privilege level is promoted (in this example, to level 0) as the processor operates at the higher privilege level of the EPC. After the EPC instruction is retired, the CPL will take on the privilege level previously represented by the EPC and therefore, this will become the new previous privilege level. For the purposes of the examiner's rejection, the CPL represents the previous privilege level and the EPC represents the current privilege level; the promotion or increasing of the privilege level is represented by the raising of the privilege level to that of the EPC.

Applicant argues that the Arora patent does not teach a call instruction including storing the first privilege level in a previous privilege level state. However, as stated in the applicant's argument, the CPL (previous privilege level, as stated by the rejection) is stored when it is increased at the time the EPC instruction is retired (page 13 of arguments). This process must occur at the call of an instruction since the operation of the system is governed by the instructions of instruction memory 36.

Applicant also argues that Arora does not teach a call instruction including storing a return address of the first page of memory or including storing the first privilege level in a previous privilege level state. However, Arora discloses performing a call instruction to a second page of memory (in the case of calling a subroutine, Col. 6, lines 62-67), the call instruction including: storing a return address to the first page of memory (in the case of calling a subroutine, the system must be able to return from the subroutine, Col. 6, line 62 - Col. 7, line 3, so that when the subroutine completes a return instruction may be executed. The return instruction requires the storage of a return address); and storing the first privilege level in a previous privilege level state (register CPL 38 stores the privilege level set by a previous instruction, Col. 4, lines 19-22).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Arora (6,393,556) in view of Jensen (5,133,058)

Regarding Claim 1, Arora discloses a method of promoting a current privilege level ("change current privilege level to a higher privilege level" Column 6, lines 46-61) of a processor of a computer system controlled by an operating system (Col. 1, lines 10-41) wherein the current privilege level controls application instruction execution in the system by controlling accessibility to the system resources (Column 1, lines 30-41), the method comprising:

performing a privilege level promotion instruction by the operating system (Column 4, lines 13-27, and Column 6, lines 46-61), the privilege promotion instruction being stored in a memory (instruction memory 36 storing a plurality of instructions... see Figure 2) wherein processing these instructions direct the processor to change the privilege level (privilege promotion instructions, see Col. 2, lines 19- 37), the privilege promotion instruction including:

reading a stored previous privilege level state (register CPL 38 stores the privilege level set by a previous instruction, Col. 4, lines 19-22 and wherein the comparing of two privilege levels requires reading of the privilege levels),

comparing the read previous privilege level state (CPL 38) to the current privilege level (comparing CPL to the instruction's privilege level, indicated by the EPC, wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49. The privilege level stored in CPL 38 is the previous privilege level since it represents a previous instruction, while the privilege level related to the EPC is the current privilege level since it represents the current instruction);

and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level..." indicates that the CPL is less privileged than the level indicated by the EPC), promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural privilege level from privilege level 3 to privilege level 0" wherein privilege level 0 is more privileged). The privilege level is promoted as the processor starts to operate at the higher privilege level indicated by the EPC. In comparing privilege levels, the stored privilege level (stored in CPL 38) must be read in the comparison process.

Arora does not teach the instruction memory 36 including a page of memory not writeable by application instructions at a first privilege level.

Jensen discloses a cache memory, 16 or 18, including various protection levels (protection and control information included in that tag fields) wherein the individual pages of the cache memory may be write or read protected (Col. 1, lines 45-54; Col. 5, lines 30-54; and Col. 6, line 55 – Col. 7, line 12). In this system, the cache memory

includes a page of memory not writeable by applications at a first privilege level since a page of the cache memory may be write protected. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to provide the protection bits, as disclosed by Jensen, since doing so allows the system to identify particular memory pages as write protected thus, preventing unauthorized modification of programming and providing security against viruses attacking the program code.

The steps of the invention must occur at the call of an instruction since the operation of the system is governed by the instructions of instruction memory 36.

Regarding Claim 6, Arora discloses a method of executing instructions in a computer system controlled by an operating system, the method comprising:

executing application instructions in a processor of the computer system at a current privilege level of the processor equal to a first privilege level, wherein the application instructions are stored in a first page of memory (the operation of the system is governed by the instructions of instruction memory 36), and wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources (Column 1, lines 30-41);

performing a call instruction to a second page of memory (in the case of calling a subroutine, Col. 6, lines 62-67), the call instruction including:

storing a return address to the first page of memory (in the case of calling a subroutine, the system must be able to return from the subroutine, Col. 6, line 62 - Col.

7, line 3, so that when the subroutine completes a return instruction may be executed. The return instruction requires the storage of a return address); and

storing the first privilege level in a previous privilege level state (register CPL 38 stores the privilege level set by a previous instruction, Col. 4, lines 19-22); and

performing a privilege promotion instruction by the operating system ("change current privilege level to a higher privilege level" Column 6, lines 46-61; Column 4, lines 13-27), the privilege promotion instruction being stored in the second page of memory (in case of the calling of a subroutine, which is stored in a separate page of memory since a return instruction is required, the EPC for the subroutine is also stored in a separate page of memory; see Col. 6, line 62 - Col. 7, line 3), the privilege promotion instruction including:

reading a stored previous privilege level state (register CPL 38 stores the privilege level set by a previous instruction, Col. 4, lines 19-22 and wherein the comparing of two privilege levels requires reading of the privilege levels),

comparing the read previous privilege level state (CPL 38) to the current privilege level (comparing CPL to the instruction's privilege level, indicated by the EPC, wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49. The privilege level stored in CPL 38 is the previous privilege level since it represents a previous instruction, while the privilege level related to the EPC is the current privilege level since it represents the current instruction);

and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level..." indicates that the CPL is less privileged than the level indicated by the EPC), promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural privilege level from privilege level 3 to privilege level 0" wherein privilege level 0 is more privileged). The privilege level is promoted as the processor starts to operate at the higher privilege level indicated by the EPC. In comparing privilege levels, the stored privilege level (stored in CPL 38) must be read in the comparison process.

Arora does not teach the instruction memory 36 including a page of memory not writeable by application instructions at a first privilege level.

Jensen discloses a cache memory, 16 or 18, including various protection levels (protection and control information included in that tag fields) wherein the individual pages of the cache memory may be write or read protected (Col. 1, lines 45-54; Col. 5, lines 30-54; and Col. 6, line 55 – Col. 7, line 12). In this system, the cache memory includes a page of memory not writeable by applications at a first privilege level since a page of the cache memory may be write protected. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to provide the protection bits, as disclosed by Jensen, since doing so allows the system to identify particular memory pages as write protected thus, preventing unauthorized modification of programming and providing security against viruses attacking the program code.

The steps of the invention must occur at the call of an instruction since the operation of the system is governed by the instructions of instruction memory 36.

Regarding Claims 12, 17 and 23 Arora discloses a computer system comprising:

a processor (Figure 2, processor 30) having current privilege level which controls accessibility to the system resources (Column 1, lines 30-41 and Column 4, lines 13-27) and having a previous privilege level state (CPL 38),

a memory (Figure 2, Instruction memory 36) storing a privilege promotion instruction ("memory stores a plurality of instructions" such as an "EPC instruction which directs the processor to change the privilege level of the architectural current privilege level", see Column 3, lines 20-25 and Column 4, lines 13-27), and an operating system stored in the memory for controlling the processor and memory (operating system instructions are assigned one privilege level…, Col. 1, lines 30-41) and performing the privilege level promotion instruction as follows:

reading a stored previous privilege level state (register CPL 38 stores the privilege level set by a previous instruction, Col. 4, lines 19-22),

comparing the read previous privilege level state (CPL 38) to the current privilege level (comparing CPL to the instruction's privilege level, indicated by the EPC, wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level, column 6, lines 46-49. The privilege level stored in CPL 38 is the previous privilege level since it represents a previous instruction,

while the privilege level related to the EPC is the current privilege level since it represents the current instruction);

and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level..." indicates that the CPL is less privileged than the level indicated by the EPC), promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural privilege level from privilege level 3 to privilege level 0" wherein privilege level 0 is more privileged). The privilege level is promoted as the processor starts to operate at the higher privilege level indicated by the EPC. In comparing privilege levels, the stored privilege level (stored in CPL 38) must be read in the comparison process.

Arora does not teach the instruction memory 36 including a page of memory not writeable by application instructions at a first privilege level.

Jensen discloses a cache memory, 16 or 18, including various protection levels (protection and control information included in that tag fields) wherein the individual pages of the cache memory may be write or read protected (Col. 1, lines 45-54; Col. 5, lines 30-54; and Col. 6, line 55 – Col. 7, line 12). In this system, the cache memory includes a page of memory not writeable by applications at a first privilege level since a page of the cache memory may be write protected. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Arora to provide the protection bits, as disclosed by Jensen, since doing so allows the system to identify particular memory pages as write protected thus, preventing

unauthorized modification of programming and providing security against viruses attacking the program code.

The steps of the invention must occur at the call of an instruction since the operation of the system is governed by the instructions of instruction memory 36.

Regarding Claims 2, 8, 13, 19, and 24, Arora discloses the method of promoting a current privilege level wherein the step of performing the privilege promotion instruction further includes: if the previous privilege level state is more privileged then the current privilege level ("if the EPC instruction specifies a privilege level lower than or the same as the architectural current privilege level…"), taking an illegal operation fault ("the processor will issue a fault", Column 6, lines 55-61).

Regarding Claims 3, 9, 14, and 20, Arora discloses the method of promoting a current privilege level wherein the system resources include system registers (architectural register set, Column 3, lines 61-67).

Regarding Claims 4, 10, 15, and 21, Arora discloses the method of promoting a current privilege level wherein the system resources include system instructions ("memory 36 stores a plurality of instructions that are processed in the pipeline", column 3, lines 22-25).

Regarding Claims 5, 11, 16, and 22, Arora discloses the method of promoting a current privilege level wherein the system resources include memory pages (Figure 2, instruction memory 36).

Regarding Claim 7, and 18, Arora discloses the method of promoting a current privilege level further comprising:

performing a return instruction including:

transferring instruction control flow to the stored return address to the first page of memory, and demoting the current privilege level to the stored previous privilege level ("a return instruction would instruct the processor to decrease the architectural current privilege level to the previous privilege level", Column 6, line 65-Column 7, line 3).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Midys Rojas/

Examiner, Art Unit 2185

/Tuan V. Thai/

Primary Examiner, Art Unit 2185